REMARKS

This Amendment is submitted in response to the Office Action dated September 7, 2006, having a shortened statutory period set to expire December 7, 2006. Applicant has submitted herewith the fee set forth in 37 CFR 1.17 to extend the period for response to January 7, 2007.

INFORMATION DISCLOSURE STATEMENT

In paragraph 2 of the present Office Action, the Examiner notes that an IDS had not been submitted as of the mailing date of the present Office Action. Applicant filed an IDS on October 16, 2003.

DRAWINGS

In paragraph 3 of the present Office Action, Figures 3A-3D, 4A-4E, 5A-5B, 6A-6B, 7 and 17 are objected to as failing to include the legend "Prior Art". In response, Applicant has proposed amendments to Figures 3A-3D, 4A-4C, 4E, 5A-5B, 6A-6B and 7 to include the legend "Prior Art", as shown in the attached replacement sheets.

Applicant respectfully traverses the objection to the figures as applied to Figures 4D and 17 and submits that these figures should not be labeled "Prior Art" because such designation would be inaccurate given the depiction therein of features that are not within the prior art. For example, Figure 4D depicts, *inter alia*, instrumentation entity proto files 460, instrumentation entity HDL files 461, instrumentation entity proto files 468, instrumentation entity proto data structures 466, and design entity HDL files 340, each of which may contain novel declarations or representations of trace array instrumentation entities as described, for example, at paragraph [0229] of the present specification. Because such trace array instrumentation entities are not taught or suggested by the prior art, Applicant respectfully submits that the designation of Figure 4D as prior art would be inaccurate. Similarly, Figure 17 depicts a novel trace file 1600 in accordance with the present invention. Because such trace files are not taught or suggested by the prior art, Applicant respectfully submits that the designation of Figure 17 as prior art would be inaccurate.

CLAIM OBJECTION

In paragraph 4 of the present Office Action, Claim 1 is objected to as containing a grammatical error. In response, Applicant has amended Claim 1 to correct the error noted by the Examiner. Applicant thanks the Examiner for his diligence in reviewing the claims.

CLAIM REJECTIONS UNDER 35 U.S.C. § 101

In paragraph 8 of the present Office Action, Claims 6-11 and 31-45 are rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter. In response, Applicant has amended Claim 6 to overcome the rejection by including the recitation "placing the simulation model in data storage," which provides a useful, tangible, and concrete result, namely, a simulation model for an electronic design residing in data storage. In addition, Applicant has amended each of Claims 31-45 to recite an apparatus rather than a "program product" to address the Examiner's concern that these claims are directed to software *per se* rather than one of the classes of statutory subject matter set forth in 35 U.S.C. § 101.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

In paragraph 9 of the present Office Action, Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner believes the specification does not enable the feature in Claim 3 of specifying an association between an enumerated value and a value of the at least one signal comprising a monitored signal set.

Applicant respectfully traverses the Examiner's position and points out that the two exemplary syntaxes described beginning at paragraph [0247] of the present specification clearly teach how a user can specify "an association between an enumerated value and a value of said monitored signal set," as now recited in Claim 3. For example, referring specifically to the HDL code sample provided in paragraph [0248], Applicant notes that lines 90 and 95 respectively associate the user-selected enumerated value Enum1 with the set of signal values b'0000' and associate the user-selected enumerated value Enum2 with the set of signal values x'F'. Because the specification clearly teaches how a user can establish a user-selected enumerated value and associate that value with a set of signal values and further provides multiple code samples

demonstrating the specification of such an association, Applicant submits that the rejection of Claim 3 under the enablement requirement of 35 U.S.C. § 112, first paragraph, is not well founded and should be withdrawn.

In paragraphs 9-10 of the present Office Action, Claims 11, 26 and 41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement and written description requirements. Specifically, the Examiner believes that the claimed feature of "automatically replicating said trace array within a plurality of instances of an entity declared by an HDL file" is not enabled or described in such a way as to demonstrate that Applicant had possession of the invention at the time the application was filed.

Applicant respectfully traverses the Examiner's position and draws the Examiner's attention to paragraph [0055] of the present specification, which introduces the concept of replication of instances of a particular entity by teaching that "multiple instantiations [or instances] of any duplicated function entities will be present." Next, in paragraph [0056] and [0057], the present specification teaches an exemplary simulation model containing two replicated instances 321a and 321b of an FXU entity 321 (a design entity), each having an associated description containing the entity name and a unique instantiation name. Paragraph [0065] further discloses that "each entity has a unique set of descendants and that each time an entity is instantiated, a unique instance of the entity and its descendants is created." Thus, the replication (i.e., instantiation of multiple instances) of an entity entails the replication not only of the parent entity, but any descendant entities that the parent entity contains.

Referring further to paragraph [0075], the present specification teaches that the instrumentation disclosed therein is created and referenced as entities referred to as "instrumentation entities." Thus, the teaching referenced above with respect to replication of entities extends to instrumentation entities, including those containing trace arrays. An example of the application of automatic replication to instrumentation entities is given in paragraph [0081], which teaches that "[f]or each [of] FXU instantiations [ ] 321a and 321b, an FXUCHK instantiation, 410 and 411 respectively, is automatically generated by the mechanism of the present invention." The mechanism referred to in paragraph [0081], namely, the implementation

of the model build process depicted in Figure 4D is then described in great detail in paragraphs [0101]-[0114].

In the written description provided in paragraphs [0101]-[0114] and in particular in paragraph [0110], the present specification provides pseudo-code enabling a person of ordinary skill in the art to make and use an augmented HDL compiler (e.g., HDL compiler 462) and/or an instrumentation load tool (e.g., instrumentation load tool 464) to process design entity proto files 345 and instrumentation entity proto files 460 (or if such proto files are not available and consistent, design entity HDL files 340 and/or instrumentation entity HDL files 460) in order to instrument a simulation model with instances of instrumentation entities (including replicated instrumentation entity instances) according to the present invention. The instrumentation entities are represented in the model build process by instrumentation entity proto data structures 466 and the individual instance(s), including replicated instances, of such entities are represented by instrumentation entity instance data structures 467. These data structures are depicted explicitly in Figure 4E among proto data structures 481 and instance data structures 482, respectively. Thus, it is the software tools employed in the model build process that "automatically replicate a trace array and associated support logic for every instance of the entity with which the trace array is associated," as described in paragraph [0229].

The above-cited portions of the present specification provide written description of and enablement for the claimed step of "automatically replicating said trace array within a plurality of instances of an entity declared by an HDL file" as recited in Claims 11, 26 and 41. Consequently, Applicant respectfully submits that the rejection of Claims 11, 26 and 41 under 35 U.S.C. § 112, first paragraph, is not well founded and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

In paragraph 11 of the present Office Action, Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for "omitting essential steps" and, in particular, for omitting the step of "simulation of the simulation model." In making this rejection, the Examiner cites MPEP 2172.01, which states in relevant part:

2172.01 Unclaimed Essential Matter [R-1]

...

> In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention. See In re Venezia, 530 F.2d 956, 189 USPQ 149 (CCPA 1976); In re Collier, 397 F.2d 1003, 158 USPQ 266 (CCPA 1968). >But see Ex parte Nolden, 149 USPQ 378, 380 (Bd. Pat. App. 1965) ("[I]t is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); Ex parte Huber, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.).<

Applicant respectfully traverses the Examiner's rejection and points out that the cited section of the MPEP discusses the failure to interrelate elements of the invention in the claim as a basis for rejection under 35 U.S.C. § 112, second paragraph, rather than a failure to recite essential steps. Moreover, Applicant points out that the step of "simulation of the simulation model" is not an essential step of Claim 1, which is directed to a "method of specifying a trace array for a simulation model in a data processing system" and not to a method of performing simulation of a simulation model. Inclusion within Claim 1 of a step directed to "simulation of the simulation model" would not be directed to the stated function of the claimed method (viz., "specifying a trace array") and therefore cannot be essential to the claimed method. Moreover, there is no teaching in the present specification that the step identified by the Examiner is an essential step to the method of Claim 1. Consequently, Applicant respectfully submits that the rejection of Claim 1 under 35 U.S.C. § 112, second paragraph, is overcome.

In paragraph 12 of the present Office Action, Claims 1-5 and, in particular, Claims 1 and 3 are further rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

With respect to Claim 1, the Examiner believes that the claim is indefinite in expressing whether the trace array or trace data "will be generated through simulation of the simulation

model." In response, Applicant has amended Claim 1 to delete the phrase found indefinite by the Examiner.

With respect to Claim 3, the Examiner believes it unclear "what 'specifying a trace array comprises specifying an association between an enumerated value and a set of values of said signals' is attempting to claim" (emphasis in original). Applicant respectfully traverses the rejection of Claim 3 under 35 U.S.C. § 112, second paragraph, because the claim language is clear and definite, particularly in light of the enabling description of the claimed subject matter found in the present specification, which is discussed in detail above. In the portion of the detailed description referenced above, the enumerated value is a user-selected value (e.g., "Enum1" or "cat") that is associated with a particular set of signal values. Because the meaning of the rejected phrase of Claim 3 would be well understood and definite to a person of ordinary skill in the art when Claim 3 is read in light of the present specification, Applicant respectfully submits that the rejection of Claim 3 is not well-founded and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. § 102

In paragraph 16 of the present Office Action, Claims 1-10, 16-25, and 31-40 are rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,581,191 to *Schubert*. That rejection is respectfully traversed, and favorable reconsideration of the claims is respectfully requested.

Applicant respectfully submits that exemplary Claim 1 is not rendered unpatentable by *Schubert* because that reference does not teach or suggest each claimed feature. For example, *Schubert* does not teach or suggest the following step of exemplary Claim 1:

> permitting a user to specify, in one or more statements in the one or more HDL files, an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, wherein specifying the instrumentation entity includes specifying a trace array within the instrumentation entity and indicating a monitored signal set including at least one signal among the plurality of signals, wherein the trace array concurrently stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model.

With respect to the above step of exemplary Claim 1, page 6 of the present Office Action cites the register scan chain formed of data-path registers described at col. 5, lines 1-8 of *Schubert*. However, the cited passage of *Schubert* fails to disclose "permitting a user to specify ... an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design" and further fails to disclose that specifying the instrumentation entity in this manner includes "specifying a trace array within the instrumentation entity" or "indicating a monitored signal set." Moreover, the cited passage of *Schubert* does not disclose a "trace array [that] stores multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model." Because the cited passage of *Schubert* does not teach or suggest each feature recited in Claim 1 as amended herein, Applicant respectfully submits that the rejection of Claim 1 and its dependent claims and similar Claims 16 and 31 and their respective dependent claims is overcome.

Claim 2 is further believed to be patentable over *Schubert* because that reference does not teach or suggest the following features of Claim 2:

> wherein said specifying a trace array comprises specifying a control signal among said plurality of signals, wherein a value of said monitored signal set is stored within the trace array only on cycles of functional operation during which the control signal is asserted.

Control signals such as that recited in Claim 2 are described in the present specification, *inter alia*, at paragraphs [0234] and [0235]. Applicant particularly notes that the Examiner's citation to *Schubert's* disclosure of a data-path register scan chains at col. 5, lines 1-8 of *Schubert* does not teach or suggest the specification of a control signal for a trace array in an HDL file as now recited in Claim 2. Accordingly, the rejection of Claim 2 and similar Claims 17 and 32 is believed to be overcome.

Claim 4 is further believed to be patentable over *Schubert* because that reference does not teach or suggest the following feature of Claim 4:

wherein said specifying said trace array comprises specifying for said trace array a particular type among a plurality of different types of trace arrays.

Exemplary types of trace arrays are described in the present specification, for example, in paragraph [0234]. As noted above, the cited portions of *Schubert* fail to disclose a trace array or the specification of a trace array as claimed. Consequently, *Schubert* also does not teach or suggest specifying the type of trace array, as now recited in Claim 4 and similar Claims 19 and 34.

Claim 5 is further believed to be patentable over *Schubert* because that reference does not teach or suggest the following feature of Claim 5:

wherein said specifying said trace array comprises specifying said trace array within an HDL file declaring a design entity.

With respect to this feature, page 6 of the present Office Action cites col. 6, lines 28-47 of *Schubert*, which mentions a conventional HDL description of an electronic circuit design but does not disclose the specification of an instrumentation entity having a trace array within an HDL file declaring a design entity. Consequently, the rejection of Claim 5 and similar Claims 20 and 35 is believed to be overcome.

Applicant respectfully submits that exemplary Claim 6 and its dependent claims are also not rendered unpatentable by *Schubert* under 35 U.S.C. § 102 (or § 103) because that reference does not teach or suggest each claimed feature. For example, *Schubert* does not teach or suggest the following step of exemplary Claim 6:

receiving one or more hardware description language (HDL) files declaring a plurality of design entities forming the electronic design, wherein the plurality of design entities includes a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design, wherein said one or more HDL files further include one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array within the instrumentation entity, and

indicating a monitored signal set including at least one signal among the plurality of signals.

With respect to the above step of exemplary Claim 6, page 7 of the present Office Action again cites *Schubert's* register scan chain formed of data-path registers, as described at col. 5, lines 1-8 of *Schubert.* However, the cited passage of *Schubert* fails to disclose "receiving ... one or more HDL files further includ[ing] one or more statements specifying an instrumentation entity that monitors at least one design entity among the one or more design entities but does not contribute to functional operation of the electronic design, specifying a trace array within the instrumentation entity, and indicating a monitored signal set." Instead, the cited passage of *Schubert* teaches conventional data-path registers forming a portion of the functional logic of an electronic design.

Moreover, the cited passage of *Schubert* does not disclose the following step of Claim 6:

> in response to receipt of the one or more HDL files, parsing and processing said one or more HDL files to generate a simulation model formed of representations of instances of the plurality of the design entities and a trace array within at least one of the instances of the plurality of design entities, wherein the trace array is configured to concurrently store multiple values for the monitored signal set obtained over multiple cycles of functional operation of the simulation model. (emphasis supplied)

With respect to this step, Applicant notes that *Schubert's* registers each store only a single value of a particular data-path signal, rather than "multiple values for the monitored signal set obtained over multiple cycles of functional operation," as now recited in Claim 6. Because the cited passage of *Schubert* does not teach or suggest each feature recited in Claim 6 as amended herein, Applicant respectfully submits that the rejection of Claim 6 and its dependent claims and similar Claims 21 and 36 and their respective dependent claims is overcome.

Turning now to the rejection of independent Claim 12 and its dependent claims, Applicant respectfully submits that exemplary Claim 12 is also not rendered unpatentable by

Schubert because that reference does not teach or suggest each claimed feature. For example, *Schubert* does not teach or suggest the following step of exemplary Claim 12:

> a simulator running a testcase against a simulation model of the electronic design, wherein:
>
> the simulation model is formed of representations of instances of a plurality of design entities,
>
> the instances of the design entities contain a plurality of signals, functional logic, and any storage elements that define functional operation of the electronic design,
>
> each instance of at least a particular design entity of the plurality of design entities contains an instance of an instrumentation entity that monitors the containing instance of the particular design entity but does not contribute to functional operation of the electronic design, and
>
> each instance of the instrumentation entity contains a trace array logically coupled to receive a monitored signal set including at least one signal among the plurality of signals

With respect to the foregoing step of Claim 12, page 7 of the present Office Action cites a number of passages of *Schubert* disclosing simulation. However, the cited passages of *Schubert* do not teach or suggest "running a testcase against a simulation model" constructed in the manner now recited in Claim 12. In particular, the cited passages of *Schubert* do not disclose the instantiation of an instrumentation entity having a trace array within instances of a particular design entity as claimed. Consequently, the rejection of Claim 12 and its dependent claims under 35 U.S.C. § 102 is believed to be overcome.

Applicant respectfully submits that the rejection of Claim 12 is also overcome because *Schubert* does not teach or suggest the following "recording" step of Claim 12:

> recording trace data for the monitored signal set within the trace array during the running of the testcase, wherein the recording includes concurrently storing within the trace array multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model.

With respect to the above step of Claim 12, page 7 of the present Office Action again cites the data-path register scan chain disclosed by *Schubert*. As noted above, the conventional scan chain disclosed by *Schubert* does not teach or suggest a trace array in an instrumentation entity that "does not contribute to the functional operation of the electronic design." Moreover, the conventional scan chain registers disclosed by *Schubert* cannot store "multiple values of the monitored signal set obtained over multiple cycles of functional operation of the simulation model." Consequently, the rejection of Claim 12 and its dependent claims under 35 U.S.C. § 102 is believed to be overcome.

The rejection of Claim 12 under 35 U.S.C. § 102 in view of *Schubert* is also overcome because that reference does not teach or suggest "exporting said trace data from said trace array in a trace file," as recited in Claim 12. With reference to this feature of Claim 12, the Examiner cites reading data-path scan chain registers as taught at col. 5, lines 6-8 of *Schubert*. However, as well known to those skilled in the art, scan chain data is read out in a serial bit string, not a "trace file" as claimed. In view of the failure of *Schubert* to disclose each feature of Claim 12, Applicant respectfully submits that the rejection of Claim 12 and its dependent claims and similar Claims 21 and 42 and their respective dependent claims in view of *Schubert* is overcome.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

In paragraph 17 of the present Office Action, Claims 11, 26, and 41 are rejected under 35 U.S.C. 103(a) as unpatentable in view of *Schubert* and the Examiner's Official Notice. That rejection is also respectfully traversed.

Applicant respectfully traverses the Examiner's Official Notice because the alleged support for the Official Notice, namely, the *#include* directive of the C++ programming language, does not teach or suggest the "automatically replicating said trace array within a plurality of instances of an entity" as asserted by the Examiner. As described by Microsoft Corporation at http://msdn2.microsoft.com/en-us/library/36k2cdd4(VS.80).aspx, "The #include directive tells the preprocessor to treat the contents of a specified file as if those contents had appeared in the source program at the point where the directive appears." The support for C++

source code reuse provided by the #include directive simply does not teach or suggest the replication of a trace array in a simulation model representing an electronic design.

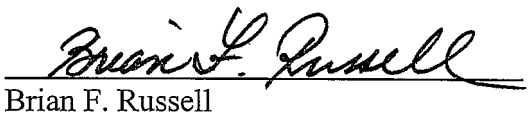
Moreover, when the knowledge in the art relied upon by the Examiner (i.e., the C++ #include directive) is viewed objectively, there is no objective teaching or suggestion of how a person of ordinary skill in the art would take this C++ programming construct and somehow modify it for application to the simulation environment of *Schubert* to obtain the invention recited in Claims 11, 26 and 41. Absent such objective teaching or suggestion found in the prior art, the rejection of Claims 11, 26 and 41 under 35 U.S.C. § 103 is not well founded and should be withdrawn.

CONCLUSION

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

A fee for a one-month extension of time is submitted herewith. No additional fee is believed to be required. If, however, any additional fees are required, please charge those fees to IBM Corporation Deposit Account No. **09-0447**.

Respectfully submitted,



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